

90nm Low-K Low Leakage Regular-Vt Standard Cells - FSD0K_A Core Cell

Key Features

- UMC's 90nm 1P9M Logic/Mixed Mode Low-K LL-RVT Process
- The 400,000 gates/mm² raw gate density offers high density needed for low cost applications
- Wide drive strength range and optimized P/N ratio for better performance
- Complete set of models for industry-standard EDA tools
- Full set of gated clock buffers for power saving
- Only Metal 1 is used in layout, each cell has at least one sub / well contact
- Flexible row abutment
- Built-in decoupling capacitance to aid IR drop in filler cells

General Description

This library is tailored for UMC's 90nm 1P9M Logic/Mixed Mode Low-K LL-RVT Process. It is especially suitable for low power / high density applications. The 10-track (2.8μm) cell height along with a wide selection of drive strengths enables customers to implement high-performance designs with smallest area. In order to maximize performance, Faraday ensures all cells have no bent-gate transistors. By following Faraday's internal evaluation procedures, this library can be customized to provide new cells to meet the special requirements from customers.

Quick Reference

	Characteristic	Description
Physical	Process	UMC 90nm 1P9M Logic/Mixed Mode Low-K LL-RVT Process
	Drawn Gate Length	0.09μm
	Gate Density	400,000 gates/mm ²
	Core Cell Height	2.8μm (10-track)
	Vertical / Horizontal Routing Grid	0.28μm / 0.28μm
	Power / ground rail width	0.68μm
	Layout resolution	0.005μm
Electrical	Recommended Operating Conditions	Power Supply Voltage: 1.08V to 1.32V Junction Temperature: -40°C ~ 125°C
	Speed	Td = 28.6ps / stage (Measured from 101-stage NAND2 ring for typical process at 1.2V and 25°C)
	Power Consumption	4.5nW / MHz / gate (Measured from NAND2 chain, output load = 2 INVERTER in typical process and operated under 1.2V, 25°C)
	Drive Strengths Level	Up to 12 (Depending on cell)

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