

## Key Features

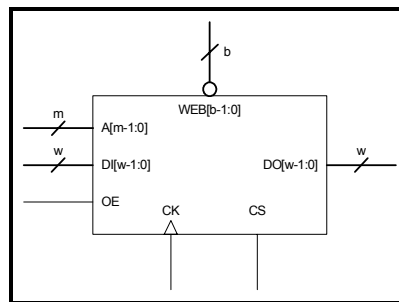
- Operating voltage range: 1.08V ~ 1.32V
- Operating junction temp. range: -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 6 metal layers
- Synchronous read and write operations
- Full custom layout density per customer configuration
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to RAM with CK rising edge
- Clocked WEB input pin to RAM with CK rising edge
- Clocked DI input pins to RAM with CK rising edge
- Byte write or word write operations available
- Verilog / VHDL timing / simulation model generator
- SPICE netlist generator
- GDSII layout generator
- Memory compiler preview UI (memaker)
- BIST code supported
- Column mux options for the best aspect ratio and speed selection

## General Description

The FSD0K\_A\_SH is a synchronous high density, single port SRAM. It is created according to UMC's 90nm 1P9M low leakage, low\_K, logic process design rules and can be incorporated with Faraday's 90nm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, FSD0K\_A\_SH compiler is capable of providing suitable synchronous RAM layout instances in minutes. It also generates data sheets, Verilog behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in the ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This provides the flexibility of CK falling edge during each operation. Both word write and byte write operations are supported.

## Symbol



## Quick Reference

Maximum Capacity	512K bits
Maximum Words	16K
Minimum Words	256
Maximum Bits	128
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Column Mux options)	4, 8, 16

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