

SYNCHRONOUS HIGH DENSITY DUAL-PORT SRAM COMPILER

Version 1.0 | August 2006

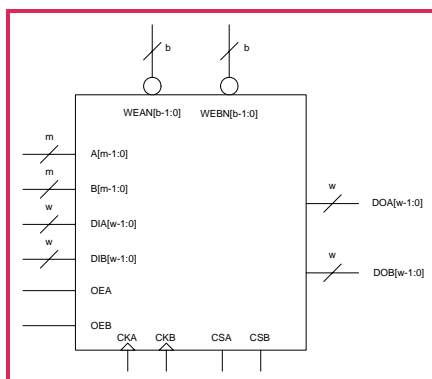
Key Features

- Synchronous read and write operations
- Low leakage device-based design
- Fully customized layout density
- Available in $1.2\text{ V} \pm 10\%$
- Automatic power-down mechanism to eliminate the DC current
- Clocked address inputs and CSA(B) to RAM at the CKA(B) rising edge
- Clocked WEA(B)N input pins to the RAM at the CKA(B) rising edge
- Clocked DIA(B) input pins to the RAM at the CKA(B) rising edge
- Supports byte/word write operations
- Verilog/VHDL timing/simulation model generators
- SPICE netlist generator
- GDSII layout database
- Memaker preview user interface
- Supports the BIST codes
- Column Mux options for the best aspect ratio

FSDOK_A_SJ is a synchronous, high density dual-port SRAM compiler. It is implemented according to UMC 90 nm logic LL-RVT (Low-K) process design rules and can be incorporated with Faraday's 90 nm standard cells. This compiler uses different combinations of words, bits, and aspect ratios that can be used to generate the most desirable configurations.

Given the desired size and timing constraints, the FSDOK_A_SJ compiler is capable of providing suitable synchronous RAM layout instances in minutes. It automatically generates the data sheets, Verilog/VHDL behavioral simulation models, SCS or ViewLogic symbols, place & route models, and test patterns to be used in the ASIC designs. The length of the duty cycle can be neglected as long as the setup and hold times and the minimum high and low pulse widths are satisfied. This allows a more flexible clock falling edge in each operation. Both word write and byte write operations are available.

Symbol Diagram



FSDOK_A_SJ

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Quick Reference

Bit cell	UMC 90 nm 8TSRAM2.08LLHVT
Cycle time	250 MHz (max.) under the worse case condition of 4K x 16
Address port	2 read/write ports
Variable capacity	512 KB (max.)
Output buffer	Tri-state
Aspect ratio (Column Mux option)	4, 8, 16
Application	Configurable SRAM modules for the embedded design on the 90 nm LL-RVT (low-K) logic process



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