

# Synchronous VIA1 Programmable ROM Compiler – FSD0K\_A\_SP

## Key Features

- Operating voltage range: 1.08V ~ 1.32V
- Operating junction temp. range : -40°C ~ 125°C
- Recommended operating ambient temp. range: 0°C ~ 85°C
- Minimum metal requirement: 6 metal layers
- Synchronous read operation
- Fully customized layout density per customer request
- Programming code by VIA1
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to ROM at CK rising edge
- Verilog / VHDL timing / simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memory compiler preview UI (Memaker)
- BIST code supported
- Multi-block options for the best aspect ratio

## General Description

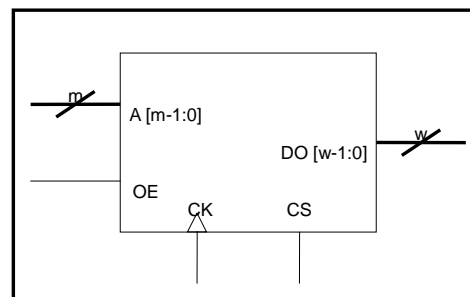
The FSD0K\_A\_SP is a synchronous VIA1 programmable ROM. It is created according to UMC's 90nm 1P9M low leakage, low\_K, logic process design rules and can be incorporated with Faraday's 90nm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, FSD0K\_A\_SP compiler is capable of providing suitable synchronous ROM layout instances in minutes. It automatically generates data sheets, Verilog behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in the ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This provides the flexibility of CK falling edge during each operation. Only one mask of VIA1 layer is needed to replace VIA1 coded ROM.

## Quick Reference

Maximum Capacity	2M bits
Maximum Words	128K
Minimum Words	512
Maximum Bits	128
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Block Mux)	1, 2, 4, 8

## Symbol



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