

90nm Standard Performance FSD0A_A 2.5V Crystal Oscillator I/O Cells

Key Features

- UMC's 90nm 1P9M Logic/Mixed Mode Low-K SP Process
- High frequency oscillator pad range: 2MHz ~ 66MHz
- Programmable output driving capability
- Oscillation mode / power down (stop) mode / tri-state mode / parallel model
- Internal feedback resistance
- Built-in antenna diodes for all pins
- ESD robustness and Latch-up immunity proven by silicon

General Description

This library is tailored for UMC's 90nm 1P9M Logic/Mixed Mode Low-K SP Process. All I/O cells have been designed as programmable crystal oscillator I/O cells. Two layout structures, both optimized for pad limited and core limited designs, are available to support each programmable feature or function.

Quick Reference

Characteristic		Description
Physical	Process	UMC 90nm 1P9M Logic/Mixed Mode Low-K SP Process
	Cell Width * Cell Height	145.6μm * 227.92μm (Staggered) 246.4μm * 142.8μm (In-line)
	Cell Layout Metal	M1, M2, M3
	Power Ring Metal	M4 and above
	Layout resolution	0.005μm
Electrical	Recommended Operating Conditions	Power Supply Voltage Core: 0.9V ~ 1.1V I/O: 2.25V ~ 2.75V
		Junction Temperature: -40°C ~ 125°C
	Frequency	High frequency oscillator pad :2M ~ 66M
	Input Threshold	CMOS

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