

90nm Low-K SP Logic Process

FSD0A_A 3.3V Analog ESD Protection Set

Key Features

- UMC's 90nm 1P9M Logic/Mixed Mode Low-K SP Process
- 3.3V ESD protection cells for analog I/O
- 3.3V Power / Ground cells with ESD protection
- Power-cut cells with ESD protection to separate 3.3V analog blocks from digital
- ESD robustness and Latch-up immunity proven by silicon

General Description

This I/O set is tailored for UMC's 90nm 1P9M Logic/Mixed Mode Low-K SP Process. This set provides a full ESD protection for an isolated analog block. Two layout structures, both optimized for pad limited and core limited designs, are available.

Quick Reference

Characteristic		Description
Physical	Process	UMC 90nm 1P9M Logic/Mixed Mode Low-K SP Process
	Cell Height	227.92 μ m (Staggered) 142.8 μ m (In-line)
	Cell Width	Multiples of X-grid (0.28 μ m)
	Cell Layout Metal	M1, M2, M3, M4
	Power Ring Metal	M4 and above
	Layout Resolution	0.005 μ m
Electrical	Recommended Operating Conditions	Power supply voltage Core: 0.9V ~ 1.1V I/O: 2.97V~3.63V
		Junction temperature: -40°C ~ 125°C

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