

# 90 NM SYNCHRONOUS HIGH DENSITY SINGLE-PORT SRAM COMPILER

## Key Features

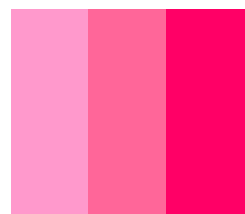
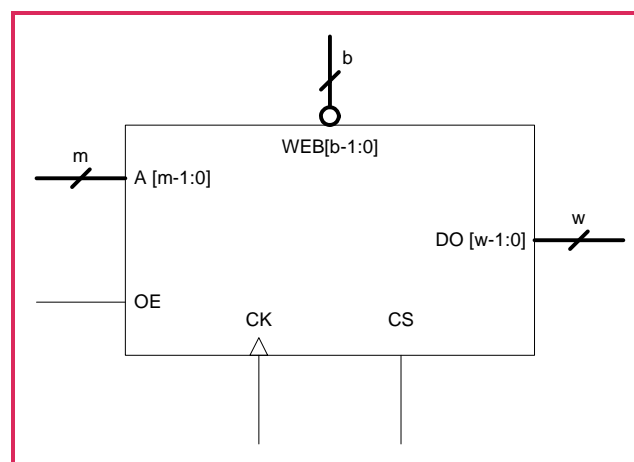
- Synchronous read and write operations
- Customized layout density per customer configuration
- High density available for 1.0 V  $\pm$ 10%
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to RAM at the CK rising edge
- Clocked WEB input pin to RAM at the CK rising edge
- Clocked DI input pins to RAM at the CK rising edge
- Byte write and word write operations available
- Verilog/VHDL timing and simulation model generator
- SPICE netlist generator
- GDSII layout generator
- Memory compiler preview UI (Memaker)
- Support BIST code
- Column multiplex options for the best aspect ratio and speed selection

## General Description

The FSD0A\_A\_SH is a synchronous high density, single-port SRAM. It is created according to UMC 90 nm logic 1P9M SP LowK process design rules and can be incorporated with Faraday 90 nm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configuration.

Given the desired size and timing constraints, the FSD0A\_A\_SH compiler is capable of providing suitable synchronous RAM layout instances in minutes. It also generates data sheets, Verilog behavioral simulation models, SCS or ViewLogic symbols, place & route models, and test patterns to be used in the ASIC designs. The duty cycle length can be neglected as long as the setup and hold time and the minimum high and low pulse widths are satisfied. It provides the flexibility of the CK falling edge at each operation. Both word write and byte write operations are supported.

## Block Diagram



# FSD0A\_A\_SH

## 90 NM SYNCHRONOUS HIGH DENSITY SINGLE-PORT

### SRAM COMPILER

#### Quick Reference

Bit Cell	UMC 90 nm 6TSRAM1.16SPHVT
Cycle Time	425 MHz (max.) under the worse case condition for 4K x 16
Address Port	1 read/write port
Variable Capacity	512k bits (max.)
Output Buffer	Tri-state
Aspect Ratio (Column Mux options)	4, 8, 16
Application	Configurable SRAM modules for embedded design using the SP LowK CMOS process

**HEADQUARTERS**

Hsinchu, Taiwan,  
Tel: 886-3-578-7888  
Fax: 886-3-578-7889  
twsales@faraday-tech.com

**USA OFFICE**

Sunnyvale, USA  
Tel: 1-408-522-8888  
Fax: 1-408-522-8889  
ussales@faraday-tech.com

**EUROPE OFFICE**

Hoofddorp, Netherlands  
Tel: 31-2356-20496  
Fax: 31-2356-36297  
eusales@faraday-tech.com

**JAPAN OFFICE**

Tokyo, Japan  
Tel: 81-3-5214-0070  
Fax: 81-3-5214-0076  
jpsales@faraday-tech.com

**CHINA OFFICE**

Shanghai, P. R. China  
Tel: 86-21-6406-7523  
Fax: 86-21-6406-5327  
cnsales@faraday-tech.com