

90 NM SYNCHRONOUS SINGLE-PORT REGISTER FILE COMPILER

Version 1.0 | April 2006

Key Features

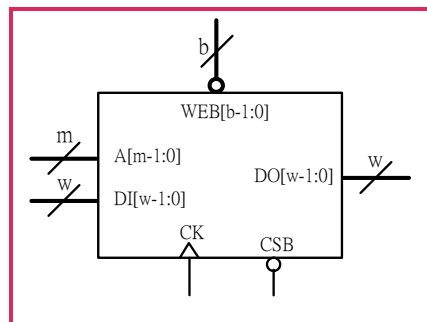
- Operating voltage range: 0.9 ~ 1.1 V
- Operating junction temp. range: -40 ~ 125 °C
- Recommended operating ambient temp. range: 0 ~ 85 °C
- Minimum metal requirement: 6 metal layers
- Synchronous read and write operations
- Fully customized layout density
- Available for 1 V ± 10 %
- Automatic power down to eliminate DC current
- Clocked address inputs and CSB to RAM with CK rising edge
- Clocked WEB input pin to RAM with CK rising edge
- Clocked DI input pins to RAM with CK rising edge
- Byte write or word write operations available
- Verilog/VHDL timing/simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memory compiler preview UI (Memaker)
- BIST code supported
- Column mux options for the best aspect ratio

General Description

The FSD0A_A_SY is a synchronous, single port register file compiler. It is implemented according to UMC's 90 nm/low-K 1P9M 1 V standard performance process design rules and can be incorporated with Faraday's 90 nm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configurations.

By requesting the desired size and timing constraints, the FSD0A_A_SY compiler is capable of providing suitable synchronous RAM layout instances in minutes. It automatically generates data sheets, Verilog/VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns used in ASIC designs. The duty cycle length can be neglected as long as the setup/hold time and minimum high/low pulse widths are satisfied. This provides the flexibility of CK falling edge during each operation. Both word write and byte write operations are supported.

Symbol



Quick Reference

Maximum Capacity	72k bits
Maximum Words	2k
Minimum Words	8
Maximum Bits	144
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Column Mux options)	2, 4, 8



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