

# Synchronous Two-Port Register File Compiler – FSD0A\_A\_SZ

## Key Features

- Operating voltage range:  
0.90V ~ 1.10V
- Operating junction temp. range:  
-40°C ~ 125°C
- Recommended operating  
ambient temp. range:  
0°C ~ 85°C
- Minimum metal requirement:  
6 metal layers
- Synchronous read and write  
operations
- Fully customized layout density
- Automatic power down to  
eliminate DC current
- Clocked address inputs and  
CSA(B)N to RAM with CKA(B)  
rising edge
- Clocked WEB input pins to RAM  
with CKB rising edge
- Clocked DI input pins to RAM  
with CKB rising edge
- Byte write or word write  
operations available
- Verilog / VHDL timing /  
simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memory compiler preview UI  
(Memaker)
- Column mux options for the best  
aspect ratio

## General Description

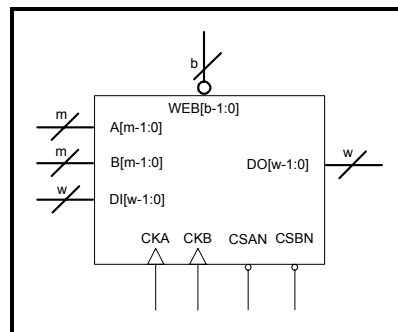
The FSD0A\_A\_SZ is a synchronous two-port register file. It is created according to UMC's 90nm 1P9M logic process design rules and can be incorporated with Faraday's 90nm standard cells. Different combinations of words, bits, and mux can be used to generate the most desirable configuration.

By requesting the desired size and timing constraints, the FSD0A\_A\_SZ compiler is capable of providing suitable synchronous RAM layout instances in minutes. It automatically generate data sheets, Verilog / VHDL behavioral simulation models, SCS or Viewlogic symbols, place & route models, and test patterns for use in ASIC designs. The duty cycle length can be neglected as long as the setup / hold time and minimum high / low pulse widths are satisfied. This allows the flexibility of a clock falling edge during each operation. Both word write and byte write operations are supported.

## Quick Reference

Maximum Capacity	72K bits
Maximum Words	2K
Minimum Words	8
Maximum Bits	144
Minimum Bits	1
Bit Increment	1
Aspect Ratio (Column Mux)	2, 4, 8

## Symbol



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