

90nm Standard Performance Low-K HVT Standard Cells - FSD0C_A Core Cell

Key Features

- UMC's 90nm 1P9M Logic/Mixed Mode Low-K HVT SP Process
- Raw gate density: 400,000 gates/mm² offers high density needed for low cost applications
- Wide drive strength range and optimized P/N ratio for performance
- Complete set of models for industry-standard EDA tools
- Full set of gated clock buffers for power saving
- Only Metal 1 used in layout, each cell has at least one sub / well contact
- Flexible row abutment
- Built-in decoupling capacitance to aid IR drop in filler cells

General Description

This library is tailored for UMC's 90nm 1P9M Logic/Mixed Mode SP Low-K HVT Process. It is especially suitable for high speed / high density applications. The 10-track (2.8μm) cell height, along with a wide selection of drive strengths enables customers to implement high performance designs with smallest area. To maximize yield, Faraday ensures all cells have no bent-gate transistors. This library can be customized to provide new cells for customers, following Faraday's internal evaluation procedures.

Quick Reference

	Characteristic	Description
Physical	Process	UMC 90nm 1P9M Logic/Mixed Mode SP Low-K HVT Process
	Drawn Gate Length	0.08μm
	Gate Density	400,000 gates/mm ²
	Core Cell Height	2.8μm (10-track)
	Vertical / Horizontal Routing Grid	0.28μm / 0.28μm
	Power / ground rail width	0.68μm
	Layout resolution	0.005μm
Electrical	Recommended Operating Conditions	Power Supply Voltage: 0.9V to 1.1V Junction Temperature: -40°C ~ 125°C
	Speed	Td = 29.9ps / stage (Measured from 101-stage NAND2 ring for typical process at 1.0V and 25°C)
	Power Consumption	4.1nW / MHz / gate (Measured from NAND2 chain, output load = 2 INVERTER in typical process and operated under 1.0V, 25°C)
	Drive Strength Levels	Up to 12 (Depending on cell)

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