

FXPLL110HD0A

PHASE LOCKED LOOP

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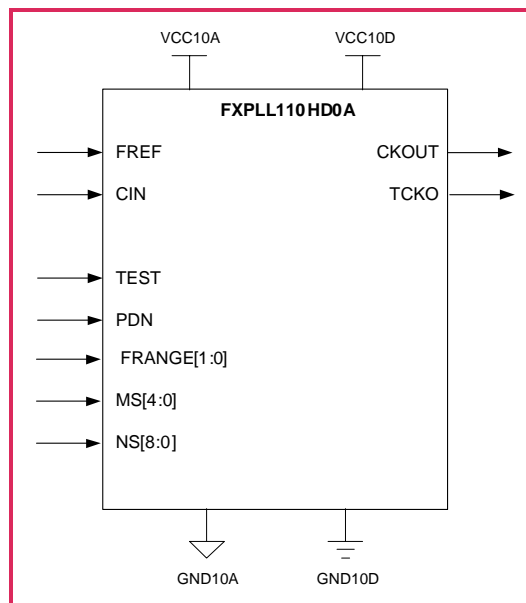
Key Features

- UMC 90 nm 1V standard logic process
- Operating voltage range: 0.9 V ~ 1.1 V
- Operating junction temperature range: -40 °C ~ 125 °C
- Minimum metal requirement: 8 metal layers
- Low jitter output
- Supports power-down and bypass modes
- Built-in loop filter

General Description

The FXPLL110HD0A is a 90 nm Phase-Locked Loop (PLL) that multiplies the external slower input signal and/or de-skews the clock. It can generate a wide range of clock frequency from 50 MHz to 1000 MHz, and the output clock is a stable, low-jitter signal. This PLL can be used in the consumer electronic products or CPU.

Symbol





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